

WHAT IS CLAIMED IS:

1. A PLL circuit comprising:

(a) a phase comparator detecting a phase difference

(b) a charge pump converting the phase difference into a voltage

5 (c) a loop filter smoothing the voltage,

(d) a voltage-controlled oscillator receiving the smoothed voltage as a control voltage, and

(e) a frequency divider frequency-dividing an output of said voltage-controlled oscillator,

10 wherein an output signal from said voltage-controlled oscillator, or frequency-divided output signal of the frequency divider, is fed back and input to said phase comparator to have its phase compared with that of an input signal;

15 (f) wherein said voltage-controlled oscillator has a non-inverting input terminal and an inverting input terminal, and a difference voltage between terminal voltages impressed upon respective ones of said non-inverting and inverting input terminals is input to said voltage-controlled oscillator as a control voltage so that said voltage-controlled oscillator will
20 oscillate at a frequency in accordance with this control voltage; and

(g) wherein said charge pump has a control unit performing control of (i) enlarging or (ii) reducing the difference voltage between both variable terminal voltages of non-inverting and

25 inverting input terminals of said voltage-controlled oscillator
in accordance with an output from said phase comparator
representing the result of the phase comparison.

2. The PLL circuit according to claim 1, wherein

said control unit for performs control of:

(i) enlarging the difference voltage by raising the
terminal voltage of the non-inverting input terminal and
5 lowering the terminal voltage of the inverting input terminal
of said voltage-controlled oscillator in accordance with the
output from said phase comparator, or

(ii) reducing the difference voltage by lowering the
terminal voltage of the non-inverting input terminal and raising
10 the terminal voltage of the inverting input terminal of said
voltage-controlled oscillator in accordance with the output
from said phase comparator.

3. The PLL circuit according to claim 1, further comprising
first and second loop filters connected at output terminals
thereof to the non-inverting and inverting input terminals,
respectively, of said voltage-controlled oscillator;

5 wherein said control unit of the charge pump performs the
following control that (i) in accordance with an output from said
phase comparator representing the result of the phase comparison,
a first capacitor a terminal voltage whereof provides an output
terminal voltage of said first loop filter is charged to thereby
10 raise the terminal voltage of the non-inverting input terminal

of said voltage-controlled oscillator, and a second capacitor
a terminal voltage whereof provides an output terminal voltage
of said second loop filter is discharged to thereby lower the
terminal voltage of the inverting input terminal of said
15 voltage-controlled oscillator, whereby the difference voltage
is enlarged at the time of an operation for raising the
oscillation frequency of said voltage-controlled oscillator;

and that (ii) in accordance with the output from said phase
comparator representing the result of the phase comparison, said
20 first capacitor is discharged to thereby lower the terminal
voltage of the non-inverting input terminal of said voltage-
controlled oscillator, and said second capacitor is discharged
to thereby raise the terminal voltage of the inverting input
terminal of said voltage-controlled oscillator, whereby said
25 difference voltage is reduced at the time of an operation to
lower the oscillation frequency of said voltage-controlled
oscillator.

4. A PLL circuit comprising:

(a) a voltage-controlled oscillator having a non-inverting
input terminal and an inverting input terminal, wherein a
difference voltage between terminal voltages impressed upon
5 respective ones of the non-inverting and an inverting input
terminals is input to said voltage-controlled oscillator as a
control voltage so that said voltage-controlled oscillator will
oscillate at a frequency in accordance with this control

voltage;

10 (b) a phase comparator comparing phase of an output signal
from said voltage-controlled oscillator, or phase of an output
signal obtained by frequency-dividing the output of said
voltage-controlled oscillator by a frequency divider, with
phase of an input signal, and outputting result of this phase
15 comparison between the output signal and the input signal;

(c) first and second loop filters connected at output
terminals thereof to the non-inverting and inverting input
terminals, respectively, of said voltage-controlled
oscillator; and

20 (d) a charge pump which includes a first circuit and a
second circuit:

(d1) the first circuit, when a signal output from said
phase comparator for raising the oscillation frequency of said
voltage-controlled oscillator is in an active state, charging
25 a first capacitor, that applies the terminal voltage of the
output terminal of said first loop filter, by a constant current
from a first constant-current source, thereby increasing the
terminal voltage at the output terminal of said first loop filter,
and discharging a second capacitor, that applies the terminal
30 voltage of the output terminal of said second loop filter, by
a constant current from a second constant-current source,
thereby decreasing the terminal voltage at the output terminal
of said second loop filter, whereby the difference voltage

across the inverting and non-inverting input terminals of said
35 voltage-controlled oscillator is enlarged; and

(d2) the second circuit, when a signal output from
said phase comparator for lowering the oscillation frequency of
said voltage-controlled oscillator is in an active state,
discharging said first capacitor, that applies the terminal
40 voltage of the output terminal of said first loop filter, by a
constant current from a third constant-current source, thereby
decreasing the terminal voltage at the output terminal of said
first loop filter, and charging said second capacitor, that
applies the terminal voltage of the output terminal of said
45 second loop filter, by a constant current from a fourth
constant-current source, thereby increasing the terminal
voltage at the output terminal of said second loop filter,
whereby the difference voltage across the inverting and non-
inverting input terminals of said voltage-controlled oscillator
50 is reduced.

5. The PLL circuit according to claim 3, wherein said charge
pump increases the terminal voltage at the output terminal of
said first loop filter by charging said first capacitor by an
output current from a transistor of a first conductivity type
5 and decreases the terminal voltage at the output terminal of said
second loop filter by charging said second capacitor by an output
current from a transistor of a second conductivity type that is
opposite the first conductivity type; and

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oscillator; and

20 (d) a first circuit, in response to receipt of a first control signal output as a result of the phase comparison by said phase comparator, supplying a first charging current (P1) from a first transistor of a first conductivity type to a capacitor of said first loop filter that supplies the terminal voltage to
25 the non-inverting input terminal of said voltage-controlled oscillator, and a first discharge current (N1) from a first transistor of a second conductivity type to a capacitor of said second loop filter that supplies the terminal voltage to the inverting input terminal of said voltage-controlled oscillator;
30 and

(e) a second circuit, in response to receipt of a second control signal output as a result of the phase comparison by said phase comparator, supplying a second charging current (P2) from a second transistor of the first conductivity type to the
35 capacitor of said second loop filter that supplies the terminal voltage to the inverting input terminal of said voltage-controlled oscillator, and a second discharge current (N2) from a second transistor of the second conductivity type to the capacitor of said first loop filter that supplies the terminal
40 voltage to the non-inverting input terminal of said voltage-controlled oscillator;

(f) whereby a ratio of a sum current (P1+N1) obtained by summing the first charging current (P1) and the first discharge

current (N1) to a sum current (P2+N2) obtained by summing the
45 second charging current (P2) and the second discharge current
(N2) is capable of being set to 1:1 independently of a difference
in output characteristics between the transistors of the first
conductivity type and the transistors of the second conductivity
type.

7. The PLL circuit according to claim 1, wherein said
voltage-controlled oscillator includes:

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5 a voltage/current conversion circuit, to which the
terminal voltage of said non-inverting input terminal and the
terminal voltage of said inverting input terminal are input as
a differential voltage, outputting a current that corresponds
to the differential input voltage; and

10 a current-controlled oscillator, to which the output
current of said voltage/current conversion circuit is input as
a control current, oscillating at a frequency conforming to this
control current.

8. A PLL circuit comprising:

5 (a) a voltage-controlled oscillator having a non-inverting
input terminal and an inverting input terminal, wherein a
difference voltage across a non-inverting and an inverting input
terminals is input to said voltage-controlled oscillator as a
control voltage so that said voltage-controlled oscillator will
oscillate at a frequency in accordance with this control
voltage;

(b) a phase comparator comparing phase of an output signal
10 from said voltage-controlled oscillator, or phase of an output
signal obtained by frequency-dividing the output of said
voltage-controlled oscillator by a frequency divider, and phase
of an input signal, outputting an UP signal for raising the
frequency of said voltage-controlled oscillator and a down
15 signal for lowering the frequency of said voltage-controlled
oscillator; and

(c) a charge pump charging and discharging capacitors based
upon the UP and DOWN signals from said phase comparator and
outputting a voltage conforming to result of the phase
20 comparison by said phase comparator;

wherein said charge pump includes:

(c1) a first switch having a control terminal
connected to the UP signal output from said phase comparator;

(c2) a first constant-current source connected
25 between one end of said first switch and a high-potential power
supply;

(c3) a first capacitor having one end connected to the
other end of said first switch and to the non-inverting input
terminal of said voltage-controlled oscillator and having its
30 other end connected to a low-potential power supply;

(c4) a second switch having a control terminal
connected to the UP signal output from said phase comparator;

(c5) a second constant-current source connected

between one end of said second switch and the low-potential power
35 supply;

(c6) a second capacitor having one end connected to
the other end of said second switch and to the inverting input
terminal of said voltage-controlled oscillator and having its
other end connected to the low-potential power supply;

40 (c7) a third switch having a control terminal
connected to the DOWN signal output from said phase comparator;

(c8) a third constant-current source connected
between the high-potential power supply and one end of said third
switch;

45 (c9) a fourth switch having a control terminal
connected to the DOWN signal output from said phase comparator;
and

(c10) a fourth constant-current source connected
between the low-potential power supply and one end of said fourth
50 switch;

(c11) wherein the other end of said third switch is
connected to one end of said second capacitor;

(c12) the other end of said fourth switch is connected
to one end of said first capacitor;

55 (d) when the UP signal output from said phase comparator
is in the active state, said first switch having the UP signal
applied to its control terminal turns on and charges said first
capacitor by a constant current from said first constant-current

source to increase the terminal voltage of said first capacitor,
60 and said second switch having the UP signal applied to its
control terminal turns on to discharge said second capacitor by
a constant current from said second constant-current source to
decrease the terminal voltage of said second capacitor, thereby
enlarging the difference voltage across the non-inverting input
65 terminal and inverting input terminal of said voltage-
controlled oscillator, whereby the oscillation frequency of
said voltage-controlled oscillator rises; and

(e) when the DOWN signal output from said phase comparator
is in the active state, said third switch having the DOWN signal
70 applied to its control terminal turns on and charges said second
capacitor by a constant current from said third constant-current
source to increase the terminal voltage of said second capacitor,
and said fourth switch having the DOWN signal applied to its
control terminal turns on to discharge said first capacitor by
75 a constant current from said fourth constant-current source to
decrease the terminal voltage of said first capacitor, thereby
reducing the difference voltage across the non-inverting input
terminal and inverting input terminal of said voltage-
controlled oscillator, whereby the oscillation frequency of
80 said voltage-controlled oscillator falls.

9. A PLL circuit comprising:

(a) a charge pump charging and discharging a capacitor in
accordance with result of a phase comparison based upon an UP

signal and a DOWM signal output from a phase comparator,

5 (b) loop filters smoothing an output voltage of said charge pump, and

(c) a voltage-controlled oscillator to which an output voltage of said loop filter is input as a control voltage, an output voltage of said voltage-controlled oscillator being fed
10 back and input to said phase comparator;

wherein

(d) an output terminal of a first loop filter and an output terminal of a second loop filter are connected to non-inverting and inverting input terminals, respectively, of said
15 voltage-controlled oscillator;

(e) said voltage-controlled oscillator has a difference voltage between terminal voltages of the non-inverting and inverting input terminals input thereto as a control voltage and oscillates at a frequency conforming to this control voltage;

20 (f) said charge pump has first to fourth constant-current sources and first to fourth current mirror circuits;

(g) when the UP signal output from said phase comparator is in the active state,

(g1) a constant current from said first constant-current
25 source is reflected by said first current mirror circuit so that a first charging current is supplied from a transistor of a first conductivity type, which forms the output terminal of said first current mirror circuit, to a capacitor of said first loop filter

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that supplies the terminal voltage to the non-inverting input
30 terminal of said voltage-controlled oscillator, and

(g2) a constant current from said second constant-current
source is reflected by said second current mirror circuit so that
a first discharge current is supplied from a transistor of a
second conductivity type, which forms the output terminal of
35 said second current mirror circuit, to a capacitor of said second
loop filter that supplies the terminal voltage to the inverting
input terminal of said voltage-controlled oscillator; and

(h) when the DOWN signal output from said phase comparator
is in the active state,

40 (h1) a constant current from said third constant-current
source is reflected by said third current mirror circuit so that
a second charging current is supplied from a transistor of the
first conductivity type, which forms the output terminal of said
third current mirror circuit, to the capacitor of said second
45 loop filter that supplies the terminal voltage to the non-
inverting input terminal of said voltage-controlled oscillator,
and

(h2) a constant current from said fourth constant-current
source is reflected by said fourth current mirror circuit so that
50 a second discharge current is supplied from a transistor of the
second conductivity type, which forms the output terminal of
said fourth current mirror circuit, to the capacitor of said
first loop filter that supplies the terminal voltage to the

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inverting input terminal of said voltage-controlled oscillator;

55 (i) whereby a ratio of a sum current obtained by summing the first charging current and the first discharge current to a sum current obtained by summing the second charging current and the second discharge current is capable of being set to 1:1 independently of a difference in output characteristics between
60 the transistors of the first conductivity type and the transistors of the second conductivity type.

10. A PLL circuit comprising:

(a) a charge pump charging and discharging a capacitor in accordance with result of a phase comparison based upon an UP signal and a DOWM signal output from a phase comparator,

5 (b) loop filters smoothing output voltages of said charge pump, and

(c) a voltage-controlled oscillator to which output voltages of said loop filters are input as control voltages,

(d) an output signal of said voltage-controlled oscillator
10 being fed back and input to said phase comparator directly, or a signal obtained by frequency-dividing the output signal of said voltage-controlled oscillator at a predetermined frequency dividing ratio being fed back and input to said phase comparator;

wherein

15 (e) first and second loop filters connected at output terminals thereof to non-inverting and inverting input terminals, respectively, of said voltage-controlled oscillator

are provided;

(f) said voltage-controlled oscillator has a difference
20 voltage between terminal voltages of said non-inverting and
inverting input terminals input thereto as the control voltage
for oscillating at a frequency in accordance with this control
voltage; and

(g) said charge pump includes:

25 (g1) a first current mirror circuit comprising first
and second transistors of a first conductivity type;

(g2) a first switch activating said first current
mirror circuit when an UP signal output from said phase
comparator is in the active state;

30 (g3) a first constant-current source connected
between an input terminal of said first current mirror circuit
and the low-potential power supply;

(g4) a second current mirror circuit comprising first
and second transistors of a second conductivity type that is
35 opposite the first conductivity type;

(g5) a second switch activating said second current
mirror circuit when the UP signal output from said phase
comparator is in the active state;

(g6) a second constant-current source connected
40 between an input terminal of said second current mirror circuit
and a high-potential power supply;

(g7) a third current mirror circuit comprising third

and fourth transistors of the first conductivity type;

(g8) a third switch activating said third current mirror circuit when the DOWN signal output from said phase comparator is in the active state;

(g9) a third constant-current source connected between an input terminal of said third current mirror circuit and the low-potential power supply;

(g10) a fourth current mirror circuit comprising third and fourth transistors of the second conductivity type;

(g11) a fourth switch activating said fourth current mirror circuit when the DOWN signal output from said phase comparator is in the active state; and

(g12) a fourth constant-current source connected between an input terminal of said fourth current mirror circuit and the high-potential power supply;

(h) the output terminal of said first current mirror circuit and the output terminal of said fourth current mirror circuit being connected in common with one end of a first capacitor a terminal voltage whereof provides an output terminal voltage of said first loop filter; and

(i) the output terminal of said second current mirror circuit and the output terminal of said third current mirror circuit being connected in common with one end of a second capacitor a terminal voltage whereof provides an output terminal voltage of said first loop filter.

11. The PLL circuit according to claim 9, wherein the transistors of the first conductivity type constituting said first and third current mirror circuits comprise P-channel MOS transistors, and the transistors of the second conductivity type
5 constituting said second and fourth current mirror circuits comprise N-channel MOS transistors.

12. The PLL circuit according to claim 10, wherein the transistors of the first conductivity type constituting said first and third current mirror circuits comprise P-channel MOS transistors, and the transistors of the second conductivity type
5 constituting said second and fourth current mirror circuits comprise N-channel MOS transistors.

13. The PLL circuit according to claim 10, wherein:

said first switch comprises a P-channel MOS transistor having a source connected to the high-potential power supply, a drain connected to a common gate of a P-channel MOS transistor
5 constituting said first current mirror circuit, and a gate connected to the UP signal from said phase comparator;

said second switch comprises an N-channel MOS transistor having a source connected to the low-potential power supply, a drain connected to a common gate of an N-channel MOS transistor
10 constituting said second current mirror circuit, and a gate connected to a signal obtained by inverting the UP signal from said phase comparator;

said third switch comprises a P-channel MOS transistor

having a source connected to the high-potential power supply,
15 a drain connected to a common gate of a P-channel MOS transistor
constituting said third current mirror circuit, and a gate
connected to the DOWN signal from said phase comparator; and

said fourth switch comprises an N-channel MOS transistor
having a source connected to the low-potential power supply, a
20 drain connected to a common gate of an N-channel MOS transistor
constituting said second current mirror circuit, and a gate
connected to a signal obtained by inverting the DOWN signal from
said phase comparator.

14. A charge pump circuit comprising:

(a) a first switch having a control terminal connected to
a first control signal;

(b) a first constant-current source connected between a
5 high-potential power supply and one end of said first switch;

(c) a first capacitor having one end connected to the other
end of said first switch and having its other end connected to
a low-potential power supply;

(d) a second switch having a control terminal connected to
10 the first control signal;

(e) a second constant-current source connected between the
low-potential power supply and one end of said second switch;

(f) a second capacitor having one end connected to the other
end of said second switch and having its other end connected to
15 the low-potential power supply;

(g) a third switch having a control terminal connected to a second control signal;

(h) a third constant-current source connected between the high-potential power supply and one end of said third switch;

20 (i) a fourth switch having a control terminal connected to the second control signal; and

(j) a fourth constant-current source connected between the low-potential power supply and one end of said fourth switch;

wherein

25 (k) the other end of said third switch is connected to one end of said second capacitor;

(l) the other end of said fourth switch is connected to one end of said first capacitor;

30 (m) when the first control signal is in the active state, said first switch turns on and supplies a constant current from said first constant-current source to said first capacitor to charge the same, and said second switch also turns on to discharge said second capacitor by a constant current from said second constant-current source, thereby enlarging a difference
35 voltage between the terminal voltage of said first capacitor and the terminal voltage of said second capacitor;

(n) when the second control signal is in the active state, said third switch turns on and supplies a constant current from said third constant-current source to said second capacitor to
40 charge the same, and said fourth switch also turns on to

discharge said first capacitor by a constant current from said fourth constant-current source, thereby reducing the difference voltage between the terminal voltage of said first capacitor and the terminal voltage of said second capacitor; and

45 (c) the terminal voltage of said first capacitor is delivered as a non-inverted output, and the terminal voltage of said second capacitor is delivered as an inverted output.

15. A charge pump circuit comprising:

(a) a first current mirror circuit comprising first and second transistors of a first conductivity type;

5 (b) a first switch having a control terminal to which a first control signal is input to activate said first current mirror circuit when the first control signal is in the active state;

10 (c) a first constant-current source connected between an input terminal of said first current mirror circuit and a low-potential power supply;

(d) a second current mirror circuit comprising first and second transistors of a second conductivity type that is opposite the first conductivity type;

15 (e) a second switch having a control terminal to which the first control signal is input to activate said second current mirror circuit when the first control signal is in the active state;

(f) a second constant-current source connected between an

input terminal of said second current mirror circuit and a
20 high-potential power supply;

(g) a third current mirror circuit comprising third and
fourth transistors of the first conductivity type;

(h) a third switch having a control terminal to which the
second control signal is input to activate said third current
25 mirror circuit when the second control signal is in the active
state;

(i) a third constant-current source connected between an
input terminal of said third current mirror circuit and the
low-potential power supply;

30 (j) a fourth current mirror circuit comprising third and
fourth transistors of the second conductivity type;

(k) a fourth switch having a control terminal to which the
second control signal is input to activate said second current
mirror circuit when the second control signal is in the active
35 state; and

(l) a fourth constant-current source connected between an
input terminal of said fourth current mirror circuit and the
high-potential power supply

wherein

40 (m) the output terminal of said first current mirror
circuit and the output terminal of said fourth current mirror
circuit are connected in common with one end of a first capacitor
the other of which is connected to the low-potential power

supply;

45 (n) the output terminal of said second current mirror circuit and the output terminal of said third current mirror circuit are connected in common with one end of a second capacitor the other end of which is connected the low-potential power supply; and

50 (o) a terminal voltage of said first capacitor is delivered as a non-inverted output and a terminal voltage of said second capacitor is delivered as an inverted output.

16. A voltage/current conversion circuit in a voltage-controlled oscillator having the voltage/current conversion circuit for converting an input voltage to a current, and a current-controlled oscillator, to which an output current from
5 said voltage/current conversion circuit is input as a control current, for oscillating at a frequency in accordance with the control current,

wherein said voltage/current conversion circuit has a non-inverting input terminal and an inverting input terminal and
10 outputs a current corresponding to a difference voltage between first and second input voltages of variable voltage values applied to said non-inverting input terminal and said inverting input terminal, respectively.

17. A PLL circuit comprising:

(a) a current-controlled oscillator generating and outputting a clock signal having a frequency conforming to an entered control current;

5 (b) a frequency divider frequency-dividing the clock signal from said current-controlled oscillator;

10 (c) a phase comparator, to which an input signal and the clock signal that is output from said frequency divider are input, outputting an UP signal and a DOWN signal in conformity with phase lag and lead of the clock signal relative to the input signal;

(d) a first charge pump for producing an output voltage by charging and discharging a capacitor based upon the UP and DOWN signals output from said phase comparator;

15 (e) a frequency comparator, to which the input signal and the clock signal that is output from said frequency divider are input, detecting a frequency error by measuring a synchronization pattern of the input signal using the clock signal output from said frequency divider;

20 (f) a second charge pump outputting an error voltage that conforms to the frequency error;

(g) a first low-pass filter to which the output voltage of said first charge pump is input;

25 (h) a second low-pass filter to which the output voltage of said second charge pump is input;

(i) a first voltage/current conversion circuit converting the output voltage of said first low-pass filter to current; and

(j) a second voltage/current conversion circuit converting the output voltage of said second low-pass filter to current;

30 wherein

(k) a sum current obtained by summing a current from said first voltage/current conversion circuit and a current from said second voltage/current conversion circuit is input to said voltage-controlled oscillator as the control current;

35 (l) said voltage/current conversion circuit has a non-inverting input terminal and an inverting input terminal and outputs a current in accordance with a difference voltage between terminal voltages of said non-inverting and inverting input terminals;

40 (m) said first low-pass filter comprises a first loop filter and a second loop filter connected at output terminals thereof to the non-inverting and inverting input terminals of said first voltage/current conversion circuit, respectively;

45 (n) said first charge pump has a control unit enlarging and/or reducing a difference voltage between the terminal voltages of the non-inverting and inverting input terminals of said voltage-controlled oscillator in which, when the UP signal is being output from said phase comparator, the control unit charges a first capacitor a terminal voltage whereof provides
50 an output terminal voltage of said first loop filter to thereby

raise the terminal voltage of the non-inverting input terminal of said voltage-controlled oscillator, and discharges a second capacitor a terminal voltage whereof provides an output terminal voltage of said second loop filter to thereby lower the terminal
 55 voltage of the inverting input terminal of said voltage-controlled oscillator, whereby the difference voltage is enlarged;

and in which, when the DOWN signal is being output from said phase comparator, the control unit discharges said first
 60 capacitor the terminal voltage whereof provides an output terminal voltage of said first loop filter to thereby lower the terminal voltage of the non-inverting input terminal of said voltage-controlled oscillator, and charges said second
 65 capacitor the terminal voltage whereof provides an output terminal voltage of said second loop filter to thereby raise the terminal voltage of the inverting input terminal of said voltage-controlled oscillator, whereby the difference voltage is reduced.

18. A PLL circuit comprising:

(a) a current-controlled oscillator generating and outputting a clock signal having a frequency conforming to an entered control current;

5 (b) a frequency divider frequency-dividing the clock signal from said current-controlled oscillator;

(c) a phase comparator, to which an input signal and the

clock signal that is output from said frequency divider are input, outputting an UP signal and a DOWN signal in conformity with
10 phase lag and lead of the clock signal relative to the input signal;

(d) a first charge pump producing an output voltage by charging and discharging a capacitor based upon the UP and DOWN signals output from said phase comparator;

15 (e) a frequency comparator, to which the input signal and the clock signal that is output from said frequency divider are input, detecting a frequency error by measuring a synchronization pattern of the input signal using the clock signal output from said frequency divider;

20 (f) a second charge pump outputting an error voltage that conforms to the frequency error;

(g) a first low-pass filter to which the output voltage of said first charge pump is input;

25 (h) a second low-pass filter to which the output voltage of said second charge pump is input;

(i) a first voltage/current conversion circuit converting the output voltage of said first low-pass filter to current; and

(j) a second voltage/current conversion circuit converting the output voltage of said second low-pass filter to current;

30 wherein

(k) a sum current obtained by summing a current from said first voltage/current conversion circuit and a current from said

second voltage/current conversion circuit is input to said voltage-controlled oscillator as the control current;

35 (l) said voltage/current conversion circuit has a non-inverting input terminal and an inverting input terminal and outputs a current in accordance with a difference voltage between terminal voltages of said non-inverting and inverting input terminals;

40 (m) said first low-pass filter comprises a first loop filter and a second loop filter connected at output terminals thereof to the non-inverting and inverting input terminals of said first voltage/current conversion circuit, respectively;

45 (n) said first charge pump has first to fourth constant-current sources and first to fourth current mirror circuits; and

50 (o) wherein when the UP signal output from said phase comparator is in the active state, a constant current from said first constant-current source is reflected by said first current mirror circuit so that a first charging current is supplied from a transistor of a first conductivity type, which forms the output terminal of said first current mirror circuit, to a capacitor of said first loop filter that supplies the terminal voltage to the non-inverting input terminal of said first voltage-controlled oscillator, and a constant current from said second constant-current source is reflected by said second current mirror circuit so that a first discharge current is supplied from

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a transistor of a second conductivity type, which forms the output terminal of said second current mirror circuit, to a capacitor of said second loop filter that supplies the terminal voltage to the inverting input terminal of said first voltage-controlled oscillator; and

(p) when the DOWN signal output from said phase comparator is in the active state, a constant current from said third constant-current source is reflected by said third current mirror circuit so that a second charging current is supplied from a transistor of the first conductivity type, which forms the output terminal of said third current mirror circuit, to the capacitor of said second loop filter that supplies the terminal voltage to the non-inverting input terminal of said first voltage-controlled oscillator, and a constant current from said fourth constant-current source is reflected by said fourth current mirror circuit so that a second discharge current is supplied from a transistor of the second conductivity type, which forms the output terminal of said fourth current mirror circuit, to the capacitor of said first loop filter that supplies the terminal voltage to the inverting input terminal of said first voltage-controlled oscillator;

(q) whereby a ratio of a sum current obtained by summing the first charging current and the first discharge current to a sum current obtained by summing the second charging current and the second discharge current is capable of being set to 1:1

independently of a difference in output characteristics between the transistors of the first conductivity type and the transistors of the second conductivity type.

19. A PLL circuit comprising:

(a) a current-controlled oscillator generating and outputting a clock signal having a frequency conforming to an entered control current;

5 (b) a frequency divider frequency-dividing the clock signal from said current-controlled oscillator;

(c) a phase comparator, to which an input signal and the clock signal that is output from said frequency divider are input, outputting an UP signal and a DOWN signal in conformity with phase lag and lead of the clock signal relative to the input signal;

(d) first charge pump producing an output voltage by charging and discharging a capacitor based upon the UP and DOWN signals output from said phase comparator;

15 (e) a frequency comparator, to which the input signal and the clock signal that is output from said frequency divider are input, detecting a frequency error by measuring a synchronization pattern of the input signal using the clock signal output from said frequency divider;

20 (f) a second charge pump outputting an error voltage that conforms to the frequency error;

(g) a first low-pass filter to which the output voltage of

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said first charge pump is input;

(h) a second low-pass filter to which the output voltage
25 of said second charge pump is input;

(i) a first voltage/current conversion circuit converting
the output voltage of said first low-pass filter to current; and

(j) a second voltage/current conversion circuit converting
the output voltage of said second low-pass filter to current;

30 wherein

(k) a sum current obtained by summing a current from said
first voltage/current conversion circuit and a current from said
second voltage/current conversion circuit is input to said
voltage-controlled oscillator as the control current;

35 (l) said voltage/current conversion circuit has a non-
inverting input terminal and an inverting input terminal and
outputs a current in accordance with a difference voltage
between terminal voltages of said non-inverting and inverting
input terminals;

40 (m) said first low-pass filter comprises by a first loop
filter and a second loop filter connected at output terminals
thereof to the non-inverting and inverting input terminals of
said first voltage/current conversion circuit, respectively;

(n) wherein said first charge pump includes:

45 (n1) a first current mirror circuit comprising first
and second transistors of a first conductivity type;

(n2) a first switch activating said first current

mirror circuit when an UP signal output from said phase comparator is in the active state;

50 (n3) a first constant-current source connected between an input terminal of said first current mirror circuit and the low-potential power supply;

(n4) a second current mirror circuit comprising first and second transistors of a second conductivity type that is
55 opposite the first conductivity type;

(n5) a second switch activating said second current mirror circuit when the UP signal output from said phase comparator is in the active state;

(n6) a second constant-current source connected
60 between an input terminal of said second current mirror circuit and a high-potential power supply;

(n7) a third current mirror circuit comprising third and fourth transistors of the first conductivity type;

(n8) a third switch activating said third current
65 mirror circuit when the DOWN signal output from said phase comparator is in the active state;

(n9) a third constant-current source connected between an input terminal of said third current mirror circuit and the low-potential power supply;

70 (n10) a fourth current mirror circuit comprising third and fourth transistors of the second conductivity type;

(n11) a fourth switch activating said fourth current

mirror circuit when the DOWN signal output from said phase comparator is in the active state; and

75 (n12) a fourth constant-current source connected between an input terminal of said fourth current mirror circuit and the high-potential power supply;

(o) wherein the output terminal of said first current mirror circuit and the output terminal of said fourth current mirror circuit being connected in common with one end of a first capacitor a terminal voltage whereof provides an output terminal voltage of said first loop filter; and

(p) wherein the output terminal of said second current mirror circuit and the output terminal of said third current mirror circuit being connected in common with one end of a second capacitor a terminal voltage whereof provides an output terminal voltage of said first loop filter.

20. A data read-out apparatus comprising:

(a) an amplifier for generating a playback RF signal, a focus error signal and a tracking error signal from data read via a head for reading data from a recording disk;

5 (b) a filter for eliminating noise from and wave-form equalizing the playback RF signal from said amplifier;

(c) a binarizing circuit for binarizing the playback RF from said filter;

(d) a PLL circuit, to which data binarized by said binarizing circuit is input, generating and outputting a read

clock synchronized to this binarized data;

(e) a demodulation circuit for demodulating data based upon the data read clock from said PLL circuit;

(f) an error correction circuit subjecting reproduced data
15 to error correction;

(g) a motor rotating said recording disk;

(h) a servo-controller controlling said head and said motor; and

(i) a CPU performing overall control of the apparatus;
20 wherein said PLL circuit is constituted by the PLL circuit set forth in claim 17.

21. A data read-out apparatus comprising:

(a) an amplifier for generating a playback RF signal, a focus error signal and a tracking error signal from data read via a head for reading data from a recording disk;

5 (b) a filter for eliminating noise from and wave-form equalizing the playback RF signal from said amplifier;

(c) a binarizing circuit for binarizing the playback RF from said filter;

(d) a PLL circuit, to which data binarized by said
10 binarizing circuit is input, generating and outputting a read clock synchronized to this binarized data;

(e) a demodulation circuit for demodulating data based upon the data read clock from said PLL circuit;

(f) an error correction circuit subjecting reproduced data

15 to error correction;

(g) a motor rotating said recording disk;

(h) a servo-controller controlling said head and said motor; and

(i) a CPU performing overall control of the apparatus;

20 wherein said PLL circuit is constituted by the PLL circuit set forth in claim 18.

22. A data read-out apparatus comprising:

(a) an amplifier for generating a playback RF signal, a focus error signal and a tracking error signal from data read via a head for reading data from a recording disk;

5 (b) a filter for eliminating noise from and wave-form equalizing the playback RF signal from said amplifier;

(c) a binarizing circuit for binarizing the playback RF from said filter;

10 (d) a PLL circuit, to which data binarized by said binarizing circuit is input, generating and outputting a read clock synchronized to this binarized data;

(e) a demodulation circuit for demodulating data based upon the data read clock from said PLL circuit;

15 (f) an error correction circuit subjecting reproduced data to error correction;

(g) a motor rotating said recording disk;

(h) a servo-controller controlling said head and said motor; and

(i) a CPU performing overall control of the apparatus;
20 wherein said PLL circuit is constituted by the PLL circuit
set forth in claim 19.

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